A COMPARISON OF THE PERFORMANCE OF THREE DIFFERENT PHASE LOCKED OSCILLATORS FABRICATED AT 21 GHZ

J. Pérez (1), P. Dorta (1), F. Sierra (2)

(1) SSR Department. ETSI. Telecomunicación. Universidad Politécnica de Madrid. Ciudad Universitaria, s/n. 28040 Madrid. SPAIN.
(2) Telecomunicación y Control, S.A., P.T.M. Tres Cantos. 28760, Madrid.

ABSTRACT

This paper describes the construction and fabrication of three different Phase Locked Oscillators (PLO) at 21 GHz. The first PLO consists of a direct division (analog and digital) from 21 GHz to the reference frequency. The second approach uses only one analog divider to reach 10.5 GHz and then a sampling phase detector. The final one consists of a 10.5 GHz MESFET Dielectric Resonator Oscillator (DRO) phase locked by means of a sampling phase detector and a multiplier (by two). A comparison of analysis, fabrication and performance of the three PLOs is presented.

INTRODUCTION

In radio-link equipments in the band from 21.2 to 23.6 GHz it is essential to have highly stable and low noise signal sources. An adequate method to obtain those synthesizers is the use of Phase Lock Loops (PLL), employing a double loop technique with a single mixer (non-harmonic) as presented in figure 1.

In order to achieve synthesizers with the desired features PLOs with excellent performances are needed. Nevertheless, beyond 20 GHz it is difficult to get direct digital microwave prescaling from the output frequency of the VCO of the PLOs. In that frequency band it is also difficult to have sample phase detectors with good performances. Taking those facts into account three possible approaches for the fabrication of PLOs have been analyzed and their performance, particularly that of phase noise, is measured. The difficulty in manufacturing these devices is also outlined.

DESCRIPTION OF THE THREE DIFFERENT APPROACHES

The three methodologies for fabricating the various PLOs are described next.

A) The first approach consists in a direct division from a 21 GHz Gunn cavity VCO to the reference frequency. Because of the fact that there are no digital dividers at 21 GHz, MESFET harmonic injection dividers were used for the first stages, and digital dividers were used in the last stages to accomplish the process of phase detection at a frequency about 100 MHz as showed in figure 2 [1-3]. The harmonic injection dividers are narrow-band devices and rather difficult to trim. However they provide the best noise performance among the various dividers [4]. Also the harmonic injection dividers do not have any problems of locking to undesired frequencies.

B) The second approach uses the same 21 GHz oscillator, as before, but requires only one analog divider to provide 10.5 GHz. The next stage is a sampling phase detector with a 100 MHz reference (the same signal as used by the PLO). This is shown in figure 3 [5]. Since the sampling phase detector replaces several dividers, it is less expensive than A). However its phase noise performance is not as good as that of A) because of the degradation in the performance due to the multiplicative processes involved. Also, this technique requires additional circuitry in order to avoid locking to undesired frequencies. This can occur if the frequency band at the input of the phase detector is higher than the reference frequency, that is, if

$$\frac{\Delta f}{N} > f_o \qquad (1)$$

where Δf is the tuning range of the VCO, N is the division factor from the output to the phase detector, and f_o is the reference frequency. In this case N=2 and f_o=100 MHz.

C) Finally, the third approach consists of a 10.5 GHz MESFET DRO that is phase locked by means of a sampling phase detector and a multiplier (by two) to obtain a 21 GHz signal as shown in figure 4. This design of the oscillator provides better phase noise performance than in the two previous cases. This approach also avoids locking problems because of its narrow bandwidth. However, some degradation in the phase noise is expected due to the multiplication at the output.

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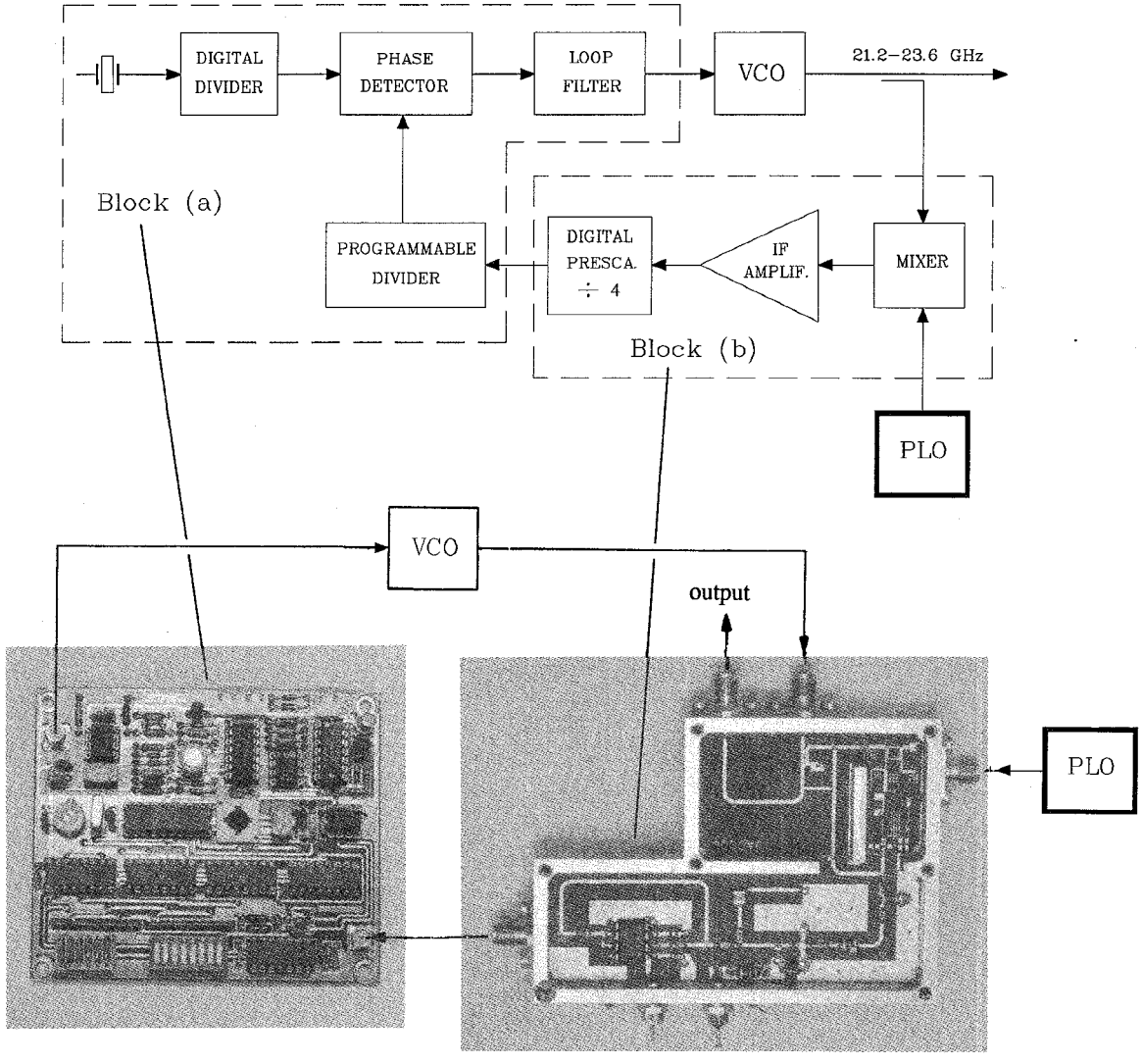

Figure 1. Scheme of the synthesizer and photographs of some blocks

The three approaches are expected to be quite similar in the phase noise at the frequencies closest to the carrier, because the multiplication factor from the reference frequency to the output frequency is the same in the three cases and the base level of thermal noise is not reached at any point of the loop.

At the offset near to the carrier the A) approach must be the best one, because it does not include any multiplication process and the additive noise of the phase detector is negligible. However in B) and C) cases the phase detector noise becames high.

Finally, at high offset from the carrier all three VCOs show similar phase noise performances. Thus the A) and B) approaches would have a similar behavior, and both of them should be better than the C) case, due to the multiplication by two used in this last approach that will produce an increment of 6 B over the VCO phase noise.

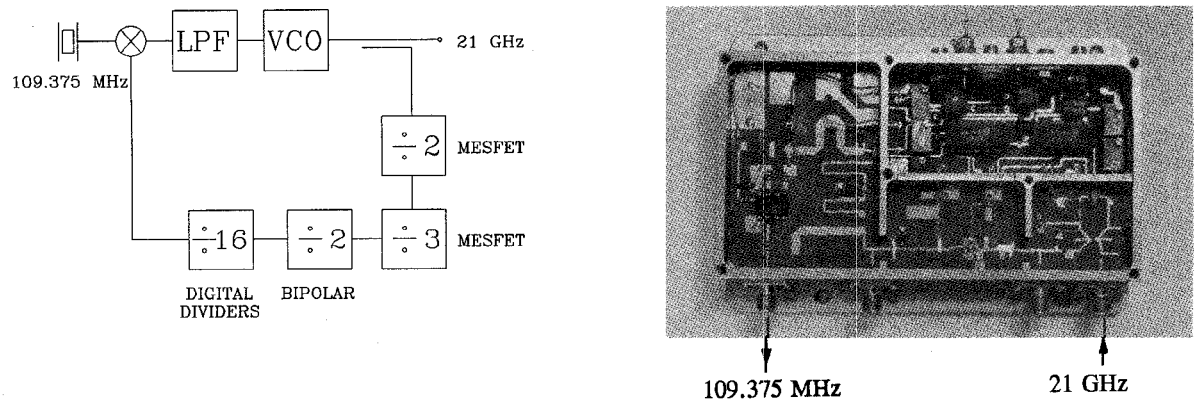

Figure 2. Approach A (direct division) and a photograph of the divider chain set

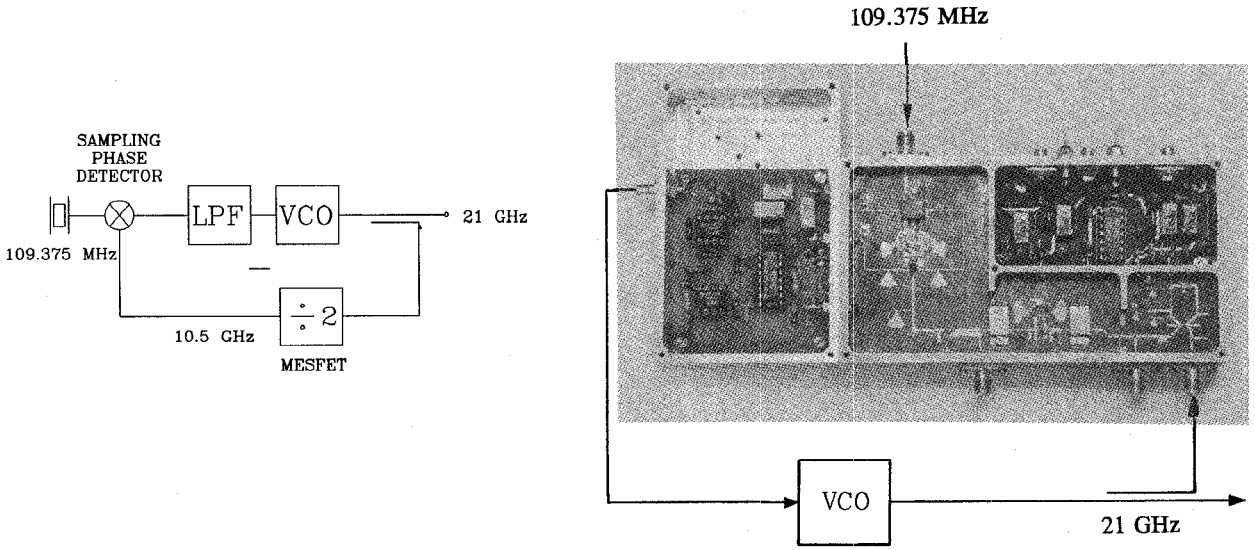

Figure 3. Approach B (one divider and sampling phase detector) and a photograph of the chain set including the divider, buffer, sampling phase detector and DC amplifier

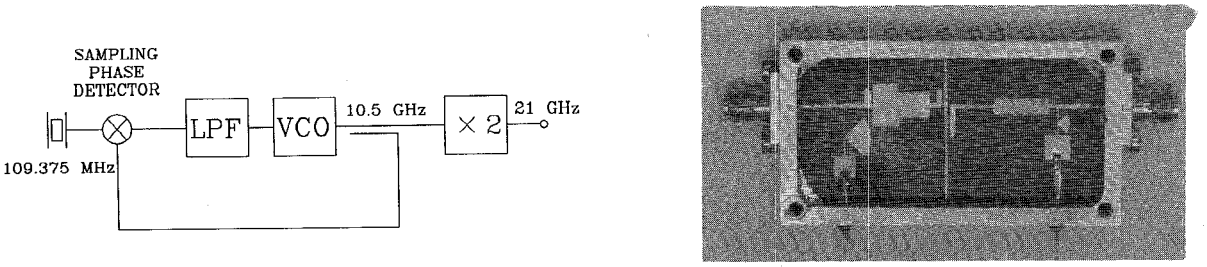

Figure 4. Approach C (sampling phase detector and multiplier) and a photograph of the multiplier chain set

EXPERIMENTAL RESULTS

The three PLOs were designed and fabricated to observe which is the cheapest and has the least problems with manufacturing. Also the simulation results are compared with the experimental data for all three approaches.

Table I summarizes the electrical performance of the three designs. The first one has the best phase noise characteristics and the least spurious response and harmonics. The third approach shows the advantage of an easy trimming. For a medium-requirement system the second design is the least expensive; in any case this approach represents an excellent compromise between the electrical performances of the other two. Thus this configuration should be adequate for a number of local oscillators in radar and communication systems; the reason for not being more widely employed may be found in the fact that very few analog dividers in the band from 20 GHz to 40 GHz are commercially available; the authors have also proposed a technique in order to obtain those dividers [1], [2].

CONCLUSIONS

Three different design and fabrication techniques for the construction of a PLO at 21 GHz is described. The relative costs and their performances have been compared and presented. Depending on the requirements, one of the three designs may be used.

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[4] M. Bomford. "Selection of Frequency Dividers for Microwave PLL Applications". Microwave Journal, November 1990, pp.159-167.

[5] Metelics Corporation. "Sampling Phase Detector (Data Sheet)".

TABLE I. PLOs PERFORMANCES

Approach	A	B	C
Phase Noise (dB/Hz)	-77 at 1 KHz -90 at 20 KHz -96 at 100 KHz	-68 at 1 KHz -80 at 20 KHz -96 at 100 KHz	-68 at 1 KHz -82 at 20 KHz -92 at 100 KHz
DC power consumption	$\simeq$7W(VCO$\simeq$3W)	$\simeq$5W(VCO$\simeq$3W)	$\simeq$7W(VCO$\simeq$0.3W)
Spurious	-61 dBc	-61 dBc	-24 dBc
Harmonics	-38 dBc	-32 dBc	-24 dBc
Trimming	difficult	normal	easy
Cost effective	medium	very good	good